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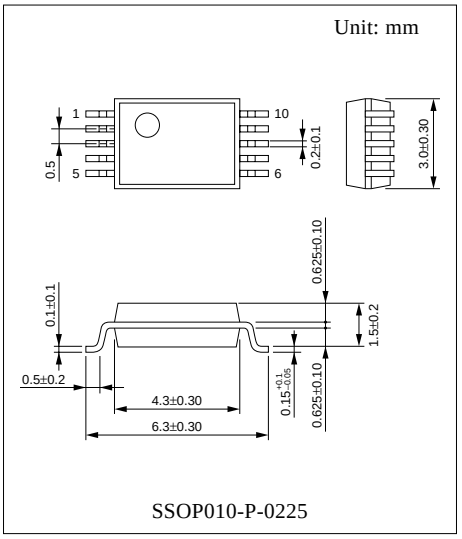
AN8016NSH

Single-channel 1.8-volt step-up DC-DC converter control IC

■ Overview

The AN8016NSH is a single-channel PWM DC-DC converter control IC that supports low-voltage operation. This IC allows a stepped-up voltage output to be provided with a minimal number of external components. It features a low minimum operating voltage of 1.8 V, and due to being provided in a 10-pin surface mount package with a 0.5 mm lead pitch, is optimal for use in miniature high-efficiency power supplies for portable equipment.



SSOP010-P-0225

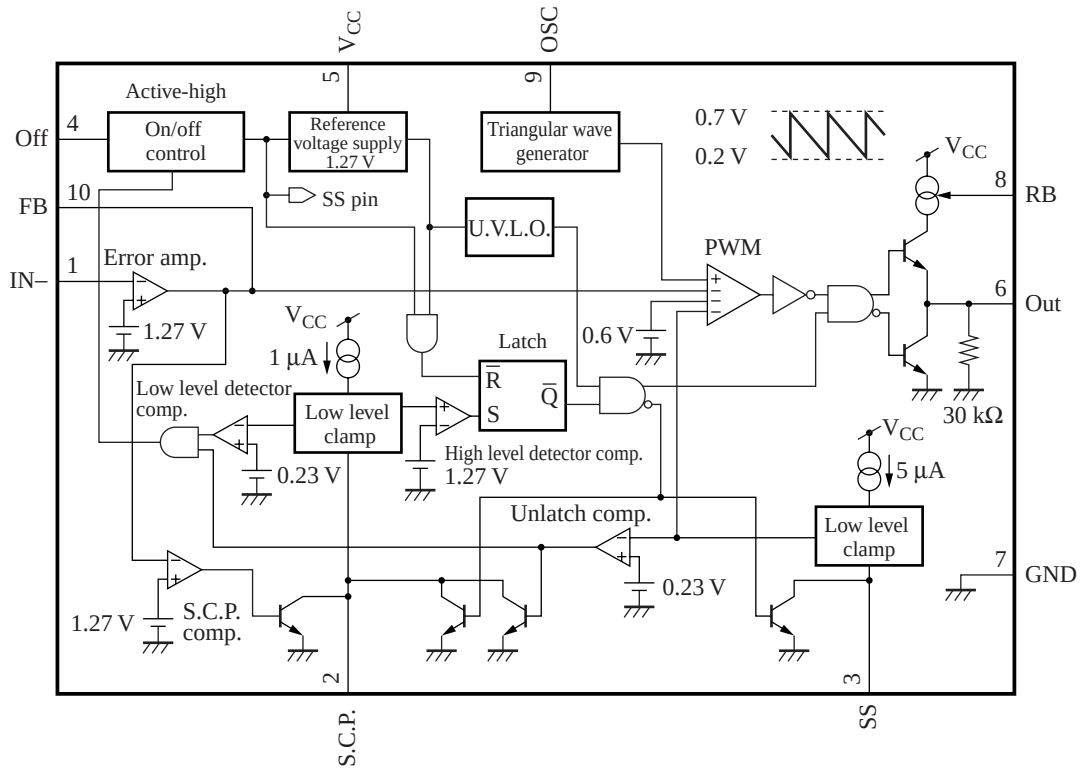
■ Features

- Wide operating supply voltage range: 1.8 V to 14 V
- High-precision reference voltage circuit: 1.27 V (allowance: ± 3%)
- Supports control over a wide output frequency range: 20 kHz to 1 MHz
- Provides a fixed output current with minimal supply voltage fluctuations by using an external resistor to set the output current with a totem pole structure in the output block.
- Large maximum output current of ± 50 mA
- Timer latch short-circuit protection circuit (charge current: 1.3 µA typical)
- Low input voltage malfunction prevention circuit (U.V.L.O.) (circuit operation start voltage: 1.6 V typical)
- On/off control function (active-high, standby current: 5 µA maximum)
- Fixed maximum duty ratio with small sample-to-sample variations (80% ± 5%)
- Adjustable soft start time provided by using separate DTC and S.C.P. pins.
- Adopts a 0.5 mm lead pitch 10 pin SO flat package (SSONF-10D)
- Adopts techniques for reducing noise, increasing the light load efficiency, and suppressing the maximum base current when turning on the npn transistor used as the external switching element.

■ Applications

- LCD displays, digital still cameras, PDAs

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description
1	IN–	Error amplifier inverting input
2	S.C.P.	Time constant capacitor connection for short-circuit protection
3	SS	Soft-start time-constant capacitor connection
4	Off	On/off control
5	V_{CC}	Supply voltage
6	Out	Push-pull output
7	GND	Ground
8	RB	Output-current setting resistor connection pin
9	OSC	Oscillator circuit timing resistor/capacitor connection pin
10	FB	Error amplifier output

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	15	V
Off pin allowable application voltage	V_{OFF}	15	V
IN– pin allowable application voltage	V_{IN-}	V_{CC}	V
Out pin allowable application voltage	V_{OUT}	15	V
Supply current	I_{CC}	—	mA
Output source current	$I_{SO(OUT)}$	–50	mA
Output sink current	$I_{SI(OUT)}$	+50	mA
Power dissipation *	P_D	115	mW
Operating temperature	T_{opr}	–30 to +85	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) 1. Currents or voltages may not be applied to any pins not stipulated above. For circuit currents, a positive (+) value indicates current flowing into the IC, and a negative (–) value indicates current flowing out of the IC.

2. Items other than the storage temperature, operating temperature, and power dissipation are all stipulated at T_a = 25°C.

3. *: T_a = 85°C. For the independent IC without a heat sink. Note that the relationship between IC power dissipation and the ambient temperature must follow the derating curve.

■ Recommended Operating Range

Parameter	Symbol	Conditions	Unit
Supply voltage	V_{CC}	1.8 to 14	V
Off control pin voltage	V_{OFF}	0 to 14	V
Output source current	$I_{SO(OUT)}$	–40 (min.)	mA
Output sink current	$I_{SI(OUT)}$	40 (max.)	mA
Timing resistance	R_T	3 to 30	kΩ
Timing capacitance	C_T	100 to 10 000	pF
Oscillator frequency	f_{OUT}	20 to 1 000	kHz
Short-circuit protection time constant setting capacitance	C_{SCP}	1 000 (min.)	pF
Output current setting resistance	R_B	0 to 10k	Ω

■ Electrical Characteristics at V_{CC} = 2.4 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
U.V.L.O. block						
Circuit operation start voltage	V_{UON}		1.45	1.6	1.75	V
Error amplifier block						
Input threshold voltage	V_{TH}	Voltage follower	1.23	1.27	1.31	V
Line regulation with input fluctuation	V_{dV}	V_{CC} = 1.8 V to 14 V	—	1.0	10	mV
Input bias current	I_B		—	0.2	1.0	μA
High-level output voltage	V_{EH}		1.85	2.0	2.15	V
Low-level output voltage	V_{EL}		—	—	0.2	V
PWM comparator block						
Output source current	I_{SS}	V_{SS} = 0.5 V	–3.5	–5	–6.5	μA
Output block						
Oscillator frequency	f_{OUT}	R_T = 12 kΩ, C_T = 330 pF	170	190	210	kHz
Maximum duty	Du_{max}		75	80	85	%
High-level output voltage	V_{OH}	I_O = –15 mA, R_B = 390 Ω	1.4	—	—	V
Low-level output voltage	V_{OL}	I_O = 10 mA, R_B = 390 Ω	—	—	0.2	V
Output source current	$I_{SO(OUT)}$	V_O = 0.9 V, R_B = 390 Ω	–45	–32	–20	mA
Output sink current	$I_{SI(OUT)}$	V_O = 0.3 V, R_B = 390 Ω	20	—	—	mA
Pull-down resistor	R_O		20	30	40	kΩ
Unlatch circuit block						
Input threshold voltage	V_{THUL}		0.13	0.20	0.27	V
Short-circuit protection circuit block						
Input threshold voltage	V_{THPC}		1.17	1.27	1.37	V
Input standby voltage	V_{STBY}		—	60	120	mV
Input latch voltage	V_{IN}		—	40	120	mV
Charge current	I_{CHG}	V_{SCP} = 0.5 V	–1.65	–1.3	– 0.95	μA
On/off control block						
Input threshold voltage	$V_{ON(TH)}$		0.8	1.0	1.3	V
Off mode SS pin voltage	$V_{OFF(SS)}$		0.13	—	0.27	V
Off mode S.C.P. pin voltage	$V_{OFF(SCP)}$		0.13	—	0.27	V
Whole device						
Average consumption current	$I_{CC(AV)}$	R_B = 390 Ω, Duty = 50%	—	3.4	5.0	mA
Latch mode consumption current	$I_{CC(LA)}$	R_B = 390 Ω	—	1.8	2.4	mA
Standby mode current	$I_{CC(SB)}$		—	—	5	μA

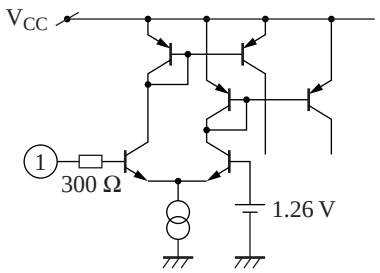
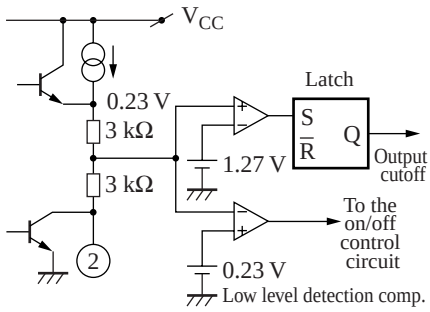
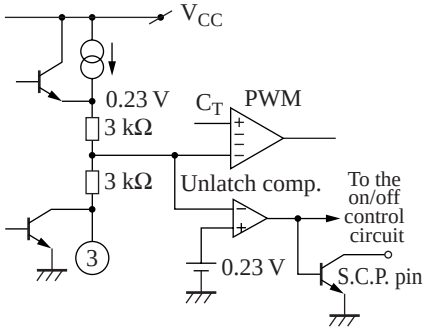
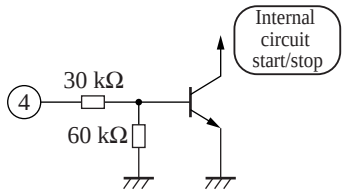
■ Electrical Characteristics at V_{CC} = 2.4 V, T_a = 25°C (continued)

• Design reference data

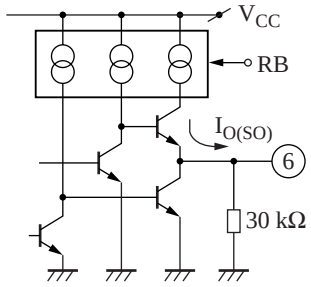
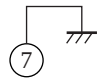
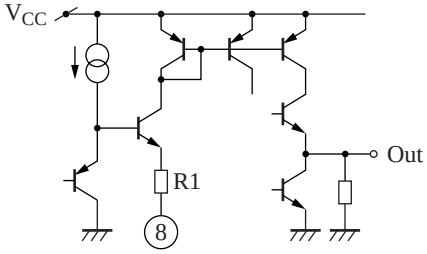
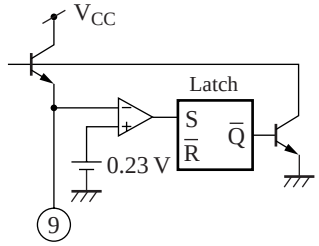
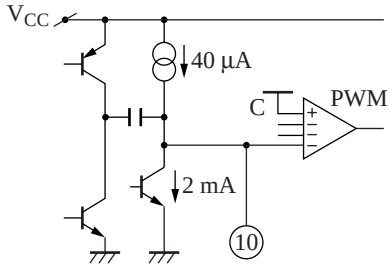
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
U.V.L.O. block						
Reset voltage	V_R			0.8		V
Error amplifier block						
V_{TH} temperature characteristics	V_{THdT}	T_a = −30°C to +85°C	− 0.5		+ 0.5	%
Output source current	$I_{SO(FB)}$	V_{FB} = 0.5 V		−40		µA
Output sink current	$I_{SI(FB)}$	V_{FB} = 0.5 V		2		mA
Open-loop gain	A_V			80		dB
PWM comparator block						
SS pin voltage	V_{SS}			1.22		V
Output block						
RB pin voltage	V_B	R_B = 390 Ω		0.13		V
Oscillator frequency supply voltage characteristics	f_{dV}	V_{CC} = 1.8 V to 14 V	−1		+1	%
Oscillator frequency temperature characteristics	f_{dT}	T_a = −30°C to 85°C	−3		+3	%
Short-circuit protection circuit block						
Comparator threshold voltage	V_{THL}			1.27		V
On/off control block						
On/Off pin current	I_{OFF}	V_{OFF} = 1.5 V		23		µA

■ Terminal Equivalent Circuits

Pin No.	Equivalent Circuit	Description	I/O
1		IN–: Error amplifier inverting input.	I
2		S.C.P.: Connection for the capacitor that sets the timer latch short-circuit protection circuit time constant. Use a capacitor with a value of 1 000 pF or higher. The charge current I_{CHG} is 1.3 µA (typical). However, the capacitor is charged with a time constant determined by 0.23 V and a resistance of 6 kΩ until the pin voltage reaches 0.23 V.	O
3		SS: Connection pin for the capacitor that determines the PWM output soft start period. Note that the the short-circuit protection circuit does not supply charge current to S.C.P. pin until this pin voltage reaches about 0.2 V. The source current I_{SS} is 5 µA (typical). However, the capacitor is charged with a time constant determined by 0.23 V and a resistor of 6 kΩ until the pin voltage reaches 0.23 V.	I
4		Off: This pin controls the on/off for the IC. High-level input: normal operation (V_{OFF} > 1.3 V) Low-level input: standby mode (V_{OFF} < 0.8 V) In the standby state, the total IC current consumption is decreased to 5 µA or under.	I
5		V_{CC}: Power supply connection. Provide an operating supply voltage of 1.8 V to 14 V.	—

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent Circuit	Description	I/O
6		Out: This is a push-pull output. The absolute maximum rating for the output current is ±50 mA. A constant-current output with excellent line regulation and minimal sample-to-sample variations can be acquired by connected an external resistor to the RB pin.	O
7		GND: IC ground.	—
8		RB: Connection for the resistor that sets the output current. Use a resistor in the range 0 to 10 kΩ. Note that the internal resistor R1 has a value of 1.0 kΩ. Thus the pin voltage will be 0.13 V when R_B is 390 Ω.	I
9		OSC: Connection for the capacitor and resistor that determines the oscillator frequency. Use a capacitor in the range 100 pF to 10 000 pF and a resistor in the range 3 kΩ to 30 kΩ. Use an oscillator frequency in the range 20 kHz to 1 MHz.	O
10		FB: Error amplifier output. A source current is about –40 µA and a sink current is about 2 mA. Correct the gain and the phase frequency characteristics by inserting a capacitor and a resistor between this pin and IN– pin.	O

■ Usage Notes

• Notes on IC power dissipation

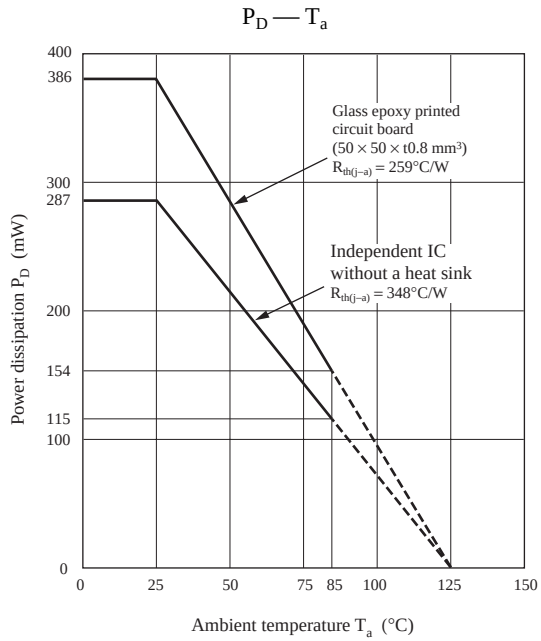
Since the power dissipation in this IC increases proportionally with the supply voltage, applications must be careful to operate so that the actual power dissipation does not exceed the power dissipation.

Since the output current set by the application circuit flows in the IC during the period corresponding to the output on duty factor (Du, where Du_{max} is 0.85), the IC power dissipation P is given by the following formula.

$$P = (V_{CC} - V_{BEQ1}) \times I_{OUT} \times Du + V_{CC} \times I_{CC} < P_D$$

■ Application Notes

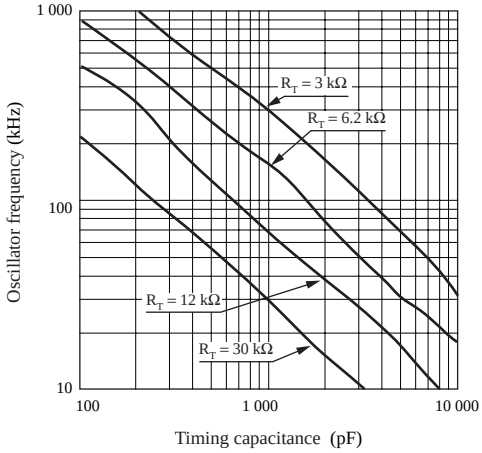
[1] Power dissipation for the SSOP010-P-0225 package



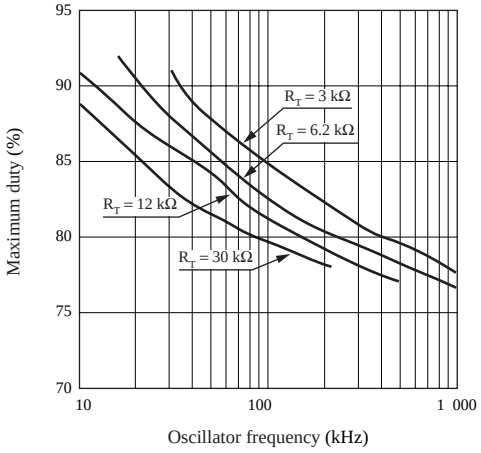
■ Application Notes (continued)

[2] Main characteristics

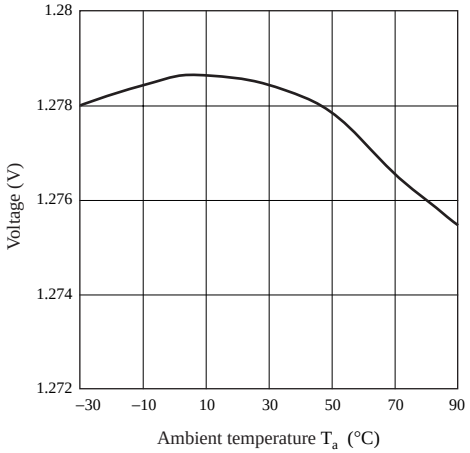
Timing capacitance — Oscillator frequency



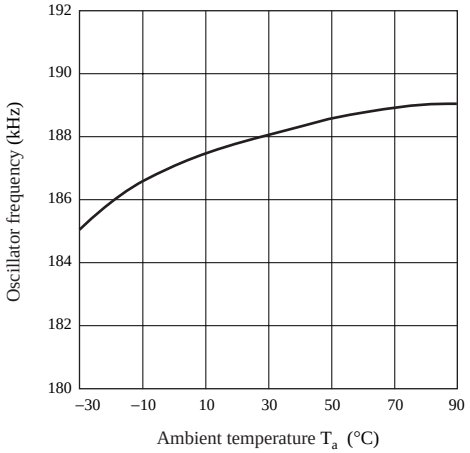
Maximum duty — Oscillator frequency



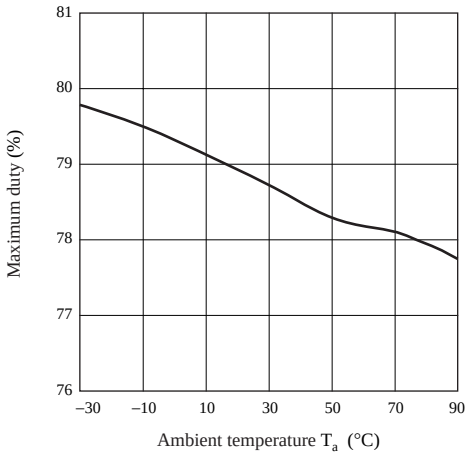
Error amplifier V_{TH} temperature characteristics



Oscillator frequency temperature characteristics



Maximum duty temperature characteristics



■ Application Notes (continued)

[3] Timing charts (internal waveforms)

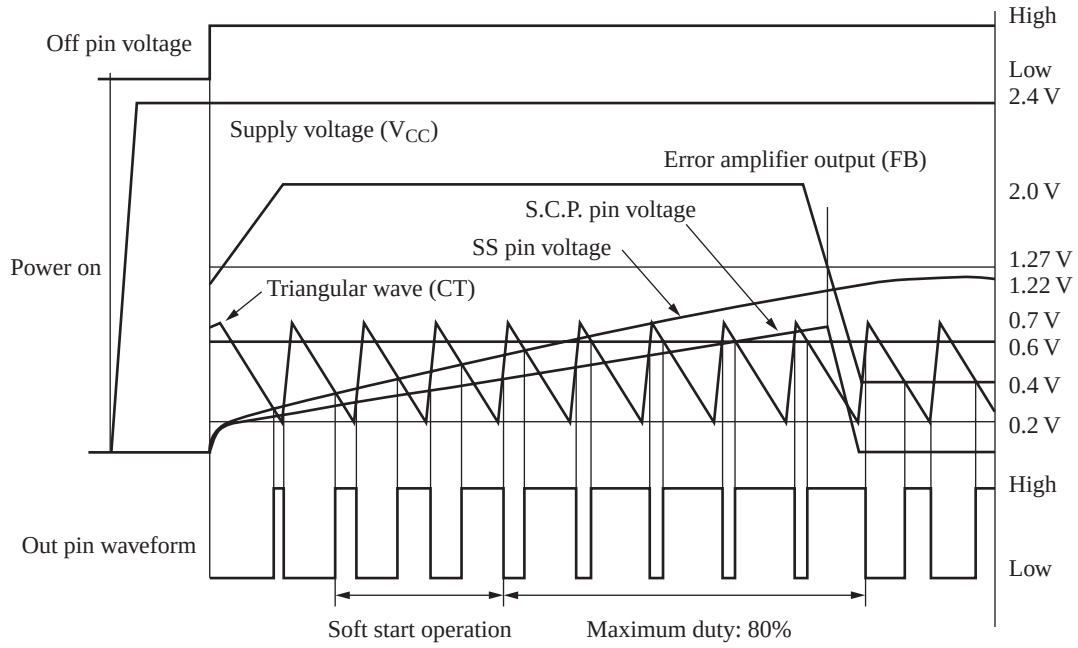


Figure 1. PWM comparator operating waveforms

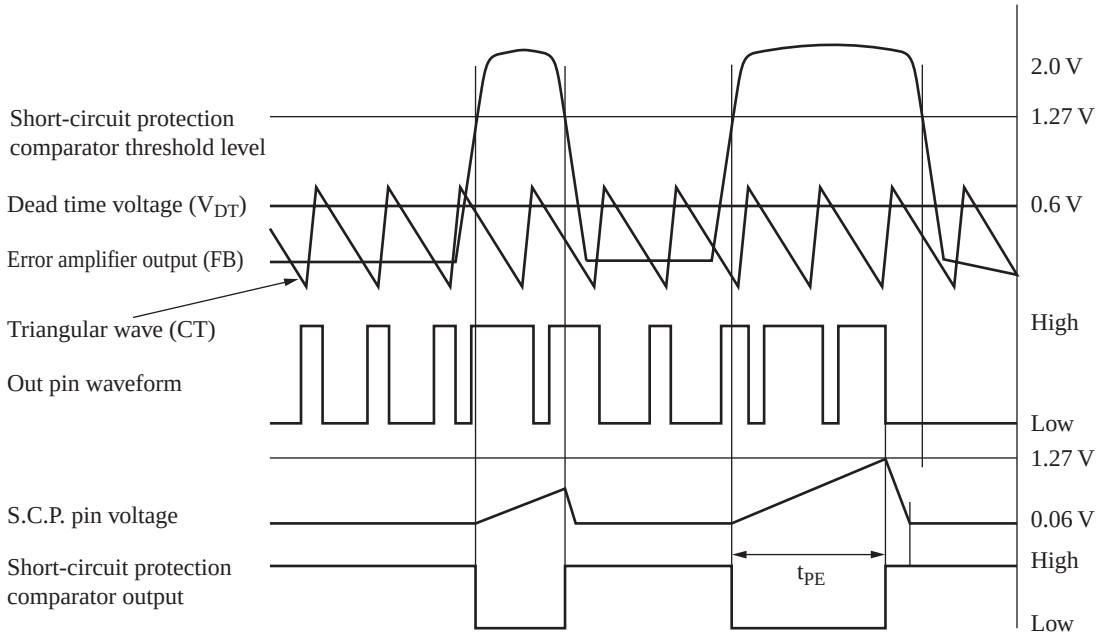


Figure 2. Short-circuit protection operating waveforms

■ Application Notes (continued)

[4] Functional descriptions

1. Reference voltage block

This circuit is composed of a band gap circuit, and outputs a 1.26-volt temperature compensated reference voltage. This reference voltage is stabilized when the supply voltage is 1.8 V or higher.

2. Triangular wave generator

This circuit generates a triangular wave like sawtooth with a peak of 0.75 V and a trough of 0.2 V using a capacitor (for the time constant) and resistor connected to the OSC pin (pin 9). The oscillator frequency can be set to any value by selecting appropriate values for the external capacitor and resistor, C_T and R_T. This oscillator can provide a frequency in the range 20 kHz to 1 MHz. The triangular wave signal is provided to the inverting input of the PWM comparator internally to the IC. Use the formulas below for rough calculation of the oscillator frequency.

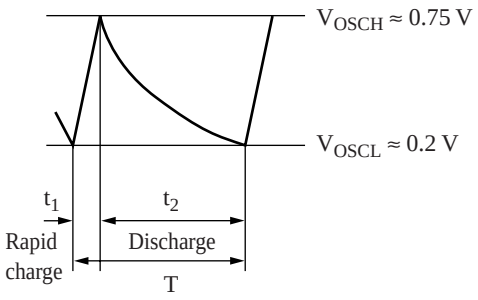


Figure 1. Triangular oscillator waveform

$$f_{OSC} \approx -\frac{1}{C_T \times R_T \times \ln \frac{V_{OSCL}}{V_{OSCH}}} \approx 0.75 \times \frac{1}{C_T \times R_T} \text{ [Hz]}$$

Note, however, that the above formulas do not take the rapid charge time, overshoot, and undershoot into account. See the experimentally determined graph of the oscillator frequency vs. timing capacitance value provided in the main characteristics section.

3. Error amplifier

This circuit is an npn-transistor input error amplifier that detects and amplifies the DC-DC converter output voltage, and inputs that signal to a PWM comparator. The 1.27 V internal reference voltage is applied to the noninverting input. Arbitrary gain and phase compensation can be set up by inserting a resistor and capacitor in series between the error amplifier output pin (pin 10) and the inverting input pin (pin 1). The output voltage V_{OUT} can be set by resistor-dividing the output as shown in figure 2.

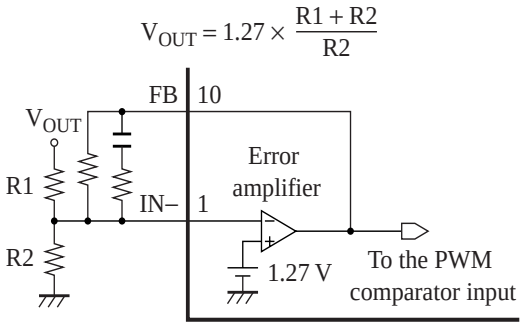


Figure 2. Connection method of error amplifier

■ Application Notes (continued)

[4] Function descriptions (continued)

4. Timer latch short-circuit protection circuit

This circuit protects the external main switching element, flywheel diode, choke coil, and other components against degradation or destruction if an excessive load or a short circuit of the power supply output continues for longer than a certain fixed period.

The timer latch short-circuit protection circuit detects the output of the error amplifiers. If the DC-DC converter output voltage drops and an error amplifier output level exceeds 1.27 V, this circuit outputs a low level and the timer circuit starts. This starts charging the external protection circuit delay time capacitor.

If the error amplifier output does not return to the normal voltage range before that capacitor reaches 1.27 V, the latch circuit latches, the output drive transistors are turned off, and the off-period is set to 100%.

5. Low input voltage malfunction prevention circuit (U.V.L.O.)

This circuit protects the system against degradation or destruction due to incorrect control operation when the power supply voltage falls during power on or power off.

The low input voltage malfunction prevention circuit detects the internal reference voltage that changes with the supply voltage level. While the supply voltage is rising, this circuit cuts off the output drive transistor until the reference voltage reaches 1.6 V. It also sets the off-period to 100%, and at the same time holds the S.C.P. pin (pin 2) and the SS pin (pin 3) at the low level.

6. PWM comparator

The PWM comparator controls the on-period of the output pulse according to its input voltage. The output transistors are turned on during periods when the OSC pin (pin 9) triangular waveform is lower than the error amplifier output pin (pin 10), the SS pin (pin 3), and the IC internally fixed dead-time voltage (about 0.6 V).

The maximum duty is fixed at 80% (typical).

The SS pin provides a constant-current source output of 5 μA (typical), and can be used to implement soft start operation in which the output pulse on period is gradually increased by connecting an external capacitor to that pin. Note that the SS pin charge operation completes when the SS pin voltage reaches 1.22 V (typical).

7. Unlatch block

The unlatch circuit holds the S.C.P. fixed at the low level while the SS pin voltage reaches the soft start operation start-level (about 0.23 V) when power is first applied. This suppresses increases in the short-circuit protection detection time associated with longer startup times.

8. Output block

The output circuit has a totem pole structure. A constant-current source output with good line regulation can be set up at an arbitrary voltage by connecting a current setting resistor to the RB pin.

This circuit can provide an output current of up to 50 mA. The output pin has a breakdown voltage of 15 V.

9. On/off control block

The IC can be turned on or off externally. When the Off pin (pin 4) voltage is set by the application of about 1.3 V or higher, the internal reference voltage is turned on, and control operation starts. If the Off pin voltage is dropped to about 0.8 V or lower, after the S.C.P. pin and SS pin external capacitors discharge, the internal reference voltage is turned off and IC control operation is stopped. This reduces IC current consumption to 5 μA or under.

■ Application Notes (continued)

[5] Time constant setup for the timer latch short-circuit protection circuit

Figure 4 shows the structure of the timer latch short-circuit protection circuit. The short-circuit protection comparator continuously compares a 1.27 V reference voltage with the error amplifier output V_{FB}.

When the DC-DC converter output load conditions are stable, the short-circuit protection comparator holds its average value, since there are no fluctuations in the error amplifier outputs. At this time, the output transistor Q1 will be in the conducting state, and the S.C.P. pin will be held at about 60 mV.

If the output load conditions change rapidly and a high-level signal (1.27 V or higher) is input to the short-circuit protection comparator's non-inverting input from the error amplifier, the short-circuit protection comparator will output a low level and the output transistor Q1 will shut off. Then, the external capacitor C_S connected to the S.C.P. pin will start to charge. When the external capacitor C_S is charged to about 1.27 V, the latch circuit will latch and the off-period will be set to 100% with the output held fixed at the low level. Once the latch circuit has latched, the S.C.P. pin capacitor will be discharged to about 40 mV, but the latch circuit will not reset unless either power is turned off or the power supply is restarted using on/off control.

The capacitor C_S is charged from 60 mV to about 230 mV with a time constant determined by a resistor of 6 kΩ, and is charged from 230 mV to 1.26 V by a constant current of about 1.3 µA.

1) $0.06 \le V_{SCP}\ [V] \le 0.23$

$$V_{SCP} = (0.23 - 0.06) \times \{1 - \exp(-\frac{t_{PE1}}{6k \cdot C_S})\}\ [V]$$

$$t_{PE1}\ [s] \approx 0.017 \times C_S\ [mF]$$

2) $0.23 \le V_{SCP}\ [V] \le 1.26$

$$1.27\ V = 0.23\ V + I_{CHG} \times \frac{t_{PE2}}{C_S}$$

$$t_{PE2}\ [s] \approx 0.80 \times C_S\ [\mu F]$$

$$\therefore\ t_{PE}\ [s] \approx t_{PE1} + t_{PE2} \approx\ 0.817 \times C_S\ [\mu F]$$

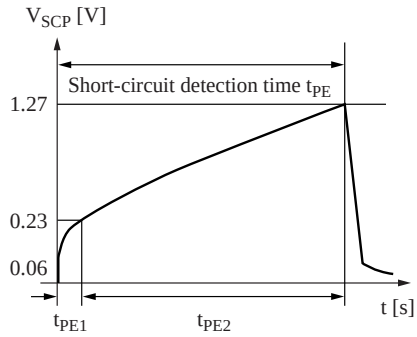


Figure 3. S.C.P. pin charging waveform

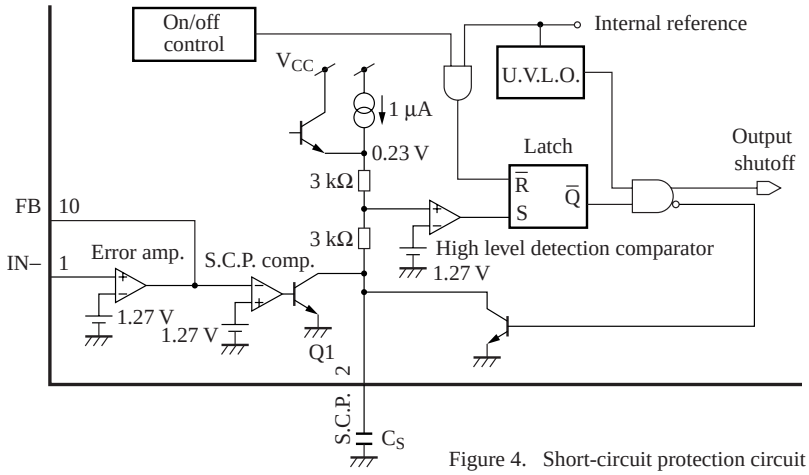


Figure 4. Short-circuit protection circuit

At power supply startup, the output appears to be in the shorted state, the error amplifier output goes to the high level, and the IC starts to charge the S.C.P. pin capacitor. Therefore, users must select an external capacitor that allows the DC-DC converter output voltage to rise before the latch circuit in the later stage latches. In particular, care is required if the soft start function is used, since that function makes the startup time longer.

■ Application Notes (continued)

[6] Setting the soft start time

A soft start function, which gradually increases the width of the output pulses at power on, will be applied if a capacitor is connected to the SS pin. This can prevent rush currents and overshoot when the power supply is turned on.

The capacitor C_{SS} is charged from 60 mV to about 230 mV with a time constant determined by a resistor of 6 kΩ, and is charged from 230 mV to 1.22 V by a constant current of about 5 μA.

The following formulas express the soft start time for the duty of up to 50%.

1) $0.06 \leq V_{SCP}\ [V] \leq 0.23$

$$V_{SCP} = (0.23 - 0.06) \times \{1 - \exp(-\frac{t_{SS1}}{6k \cdot C_S})\}\ [V]$$

$$t_{PE1}\ [s] \approx 0.017 \times C_S\ [mF]$$

2) $0.23 \leq V_{SCP}\ [V] \leq 1.26$

$$0.52\ V = 0.23\ V + I_{CHG} \times \frac{t_{SS2}}{C_S}$$

$$t_{PE2}\ [s] \approx 0.058 \times C_S\ [\mu F]$$

$$\therefore\ t_{SS}\ [s] \approx t_{SS1} + t_{SS2} \approx\ 0.075 \times C_S\ [\mu F]$$

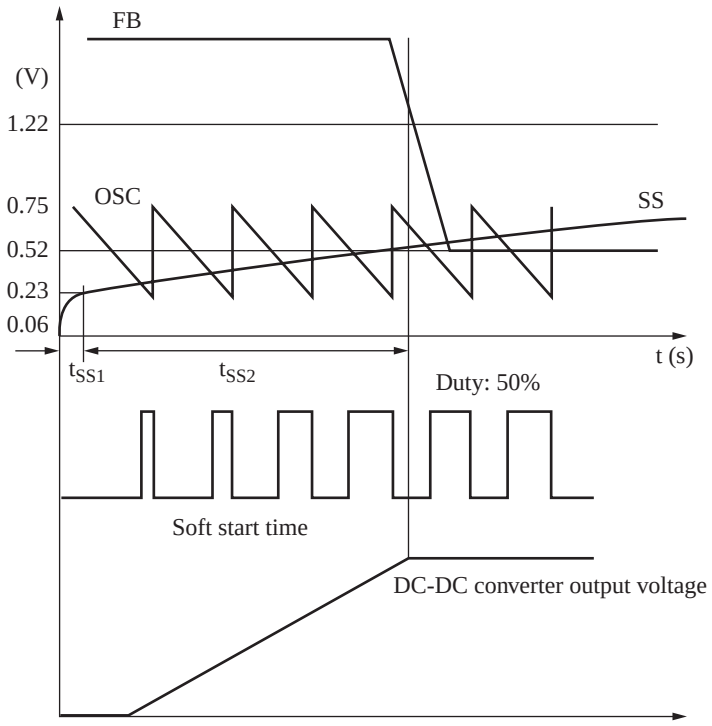


Figure 5. Soft start operating waveforms

■ Application Notes (continued)

[7] Parallel synchronous operation of multiple ICs

Multiple instances of this IC can be operated in parallel. All the ICs will operate at the same frequency if the master and slave IC OSC pins (pin 9) are connected directly.

1. Notes on S.C.P. operation during parallel operation

In the circuit in figure 6, if either the IC operating in master mode or the IC in slave mode detects a short circuit, the IC that detected the short circuit will enter latched mode. The latched mode state is a state in which the output is shut off and both the RB pin and the SS pin are set to the low level. However in this mode, this IC has an added function that holds the OSC pin at the high level (about 0.8 V).

When OSC pin of the IC that did not enter latched mode goes to the high level, the internally fixed dead- time voltage (about 0.6 V) will then be lower than the OSC pin voltage, and internal PWM circuit output will stop. That will cause this IC to go to the output shorted state, and then, this IC will also switch to latched mode.

Therefore, applications that require parallel synchronous operation should adopt the basic circuit structure shown in figure 6.

2. Usage notes

1) If capacitors are shared as shown in figure 7 to reduce the number of external components:

- The charge current will be doubled.
- The short-circuit protection circuit will not operate if the S.C.P. pin capacitor is shared.

In this circuit, even if the master IC detects a short circuit, the slave IC will not detect that state, so the S.C.P. pin will remain fixed at the low level state. Note that as a result, the short-circuit protection circuit will not operate and the IC will continue to operate at the maximum duty drive.

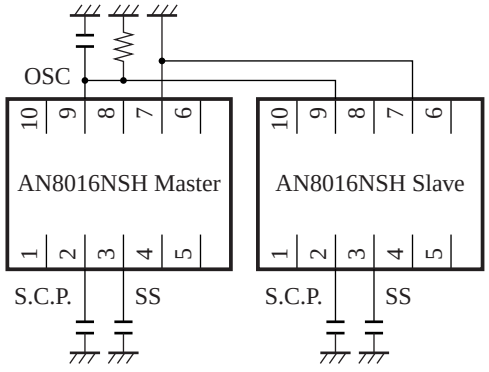


Figure 6. Slave operation circuit example

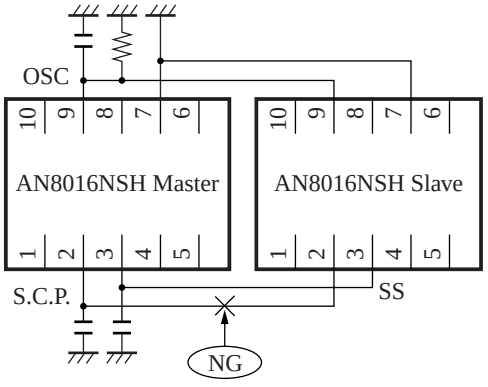
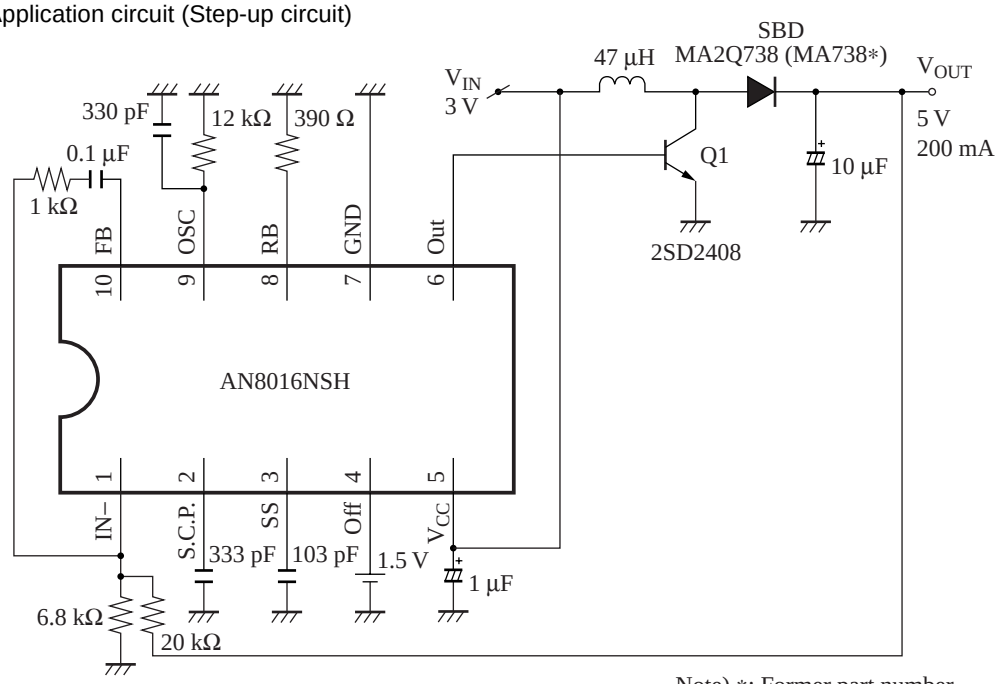


Figure 7. Slave operation circuit example

2) Note that it is not possible to operate this IC (the AN8016NSH) with the two-channel AN8017SA/AN8018SA together in parallel synchronous mode.

■ Application Circuit Examples

[1] Application circuit (Step-up circuit)



Note) ∗: Former part number

The figure shows a step-up circuit that converts a 3 V input to a 5 V output.

The AN8016NSH output stage has a totem pole circuit configuration, and can directly drive an n-channel MOSFET while minimizes switching loss and increasing efficiency. In this case, replace the npn transistor with an n-channel MOSFET in above circuit.

[2] Notes on direct n-channel MOSFET drive

1. Select an n-channel MOSFET with a low input capacitance.

   The AN8016NSH was designed to drive bipolar transistors, and adopts a circuit structure that can provide a constant-current (50 mA maximum) output source current. Furthermore, it has a sink current capacity of about 50 mA. This means that designs must be concerned about increased power dissipation due to increased rise and fall times. If problems occur, an inverter may be inserted as shown in figure 1 to provide amplification.

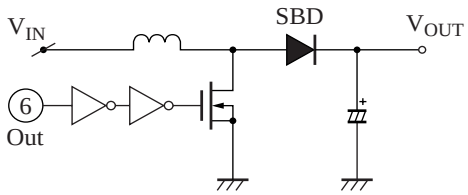
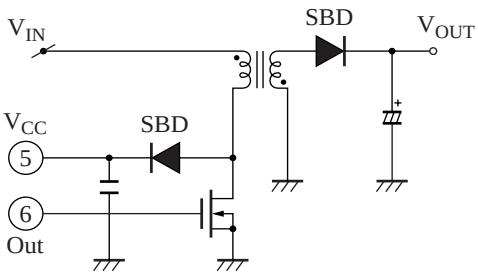


Figure 1. Output boosting circuit

2. Use an n-channel MOSFET of a low gate threshold voltage.

   Since the AN8016NSH Out pin high-level output voltage is $V_{CC} - 1.0$ V (minimum), a low V_T MOSFET with an adequately low on-resistance must be used. Also, if a large V_{GS} is required, one solution is to use a transformer as shown in figure 2, and apply a voltage of twice the input voltage to the IC's V_{CC} pin.



$$V_{CC} \approx 2 \times V_{IN} - V_D$$

Figure 2. Gate drive voltage boosting technique

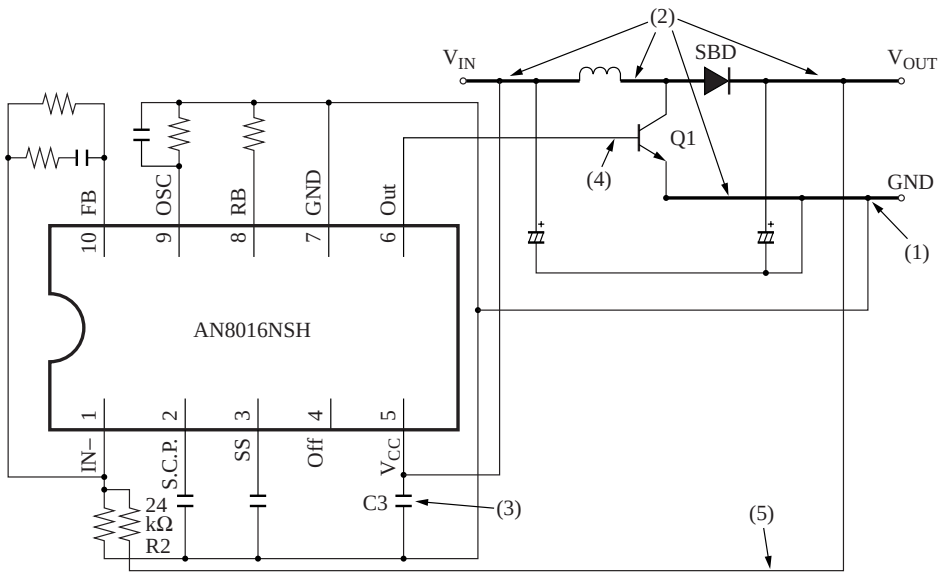
■ Application Circuit Examples (continued)

[2] Notes on direct n-channel MOSFET drive (continued)

3. Notes on printed circuit board pattern layout

Observe the following recommendations on printed circuit board pattern layout to achieve low noise and high efficiency.

1) Use extremely wide lines for the ground lines, and isolate the IC ground from the power system ground.
2) Make the lines in the high-current system as wide as possible.
3) Position the input filter capacitor C3 as close as possible to the V_{CC} and ground pins, and assure that there are no other paths for switching noise to enter the IC.
4) Keep the length of the line between the Out pin and the switching device (either a MOSFET or other transistor) as short as possible to provide a clean switching waveform to the switching device.
5) Use a relatively long line for the low-impedance side of the output voltage detection resistor R2.



[3] Evaluation board